Description

Circuit and method for clock synchronization

Telecommunication devices, such as Media Gateways typically use interworking devices to connect a packet-oriented data traffic network to a network for which voice and data transmission are based on a Time Division Multiplex TDM. For as long as these networks are to be operated alongside each other and are to be intermeshed with one another, the quality of the voice and/or data transmission between the networks is governed by the synchronicity of the two networks.

Fig. 1 shows a schematic diagram of a network interworking unit NUE. This interworking unit NUE is for example subdivided into a first network unit NTDM for which data transmission is based on Time Division Multiplex operation and a second network unit NP, a packet-oriented network unit, as well as a system control unit SS controlling the relevant firmware of the first and second network units NTDM, NP. The Time Division Multiplex network unit NTDM is subdivided into a plurality of interface units S1,...,Sn. An interface unit Sn features devices such as a clock recovery unit CR, a control register KR, a firmware module FWM, a clock selector T and also bus drivers BT. On the input side Primary Digital Carrier signals PDC1,...,n are applied to the clock recovery unit CR. 2048kBit/s and 1544kBit/s can be used as bit rates for the Primary Digital Carrier signals PDC. Fig. 2 depicts a block diagram of a data, alarm and clock recovery unit FALC which can be employed as a clock recovery unit CR in the interworking unit NUE With this clock recovery unit CR the clock signal featuring a clock frequency is obtained from the Primary Digital Carrier signals PDCn present on the input side by a digital clock recovery module CRM in each case and any

link jitter for example is filtered out of the signal by a downstream filter module JA.

Usually the interface unit Sn is embodied so that only one clock signal, which can also be referred to as a reference signal, is selected by the clock recovery unit CR from the data stream. This reference clock signal RCLK is transmitted redundantly in each case via a first bus connection REFBUS, as well as via a second redundant connection to a clock generation unit T featuring a Phase-Locked Loop PLL to a packet hub PHUB in the second unit NP.

The extracted reference clock signal RCLK(n) is pre-selected by the appropriate interface unit S1,...,Sn and forwarded by a bus driver BT. The bus driver BT operates in open collector mode in which only the low potential of the digital channel signal is applied to the bus. By contrast with the standardized collision detection bus method, as is employed in the Ethernet, a higher-ranking system control unit SS ensures here that only one bus driver DT is ever active at the same time in the interface units S1,...,Sn. The reason for this is the necessity for a real time transmission of the extracted clock or reference clock signals in unrestricted bandwidth.

The packet-oriented network unit NP features the packet hub PHUB, units such as a firmware module FWM and a clock generation unit T embodied with a Phase-Locked Loop unit PLL. The firmware module FWM of the network units NTDM and NP is activated by a system control unit SS of the interworking unit NUE.

A disadvantage of the known interworking unit NUE lies in the great effort involved in adapting the firmware if changes as regards synchronization are to be made in the first or second network unit.

The object of the invention is to specify a further circuit and a method for clock synchronization.

The object is achieved by the features of claims 1 and 13.

The invention provides the advantage of giving greater flexibility for changes to the network concerned or when networks are expanded.

The invention provides the advantage that an independent sending of clock signals from a number of clock recovery units is undertaken on a first connection without the involvement of a central control unit synchronizing the first and second network unit.

The invention provides the advantage of a coordinated pulse distance and pulse width encoding allowing a simultaneous, collision-free real time transmission of a number of plesiochronous clock signals on a common bus signal at the same time without restricting the bandwidth.

The invention provides the advantage that the firmware for activation of the interface unit as well as a synchronization of the interface unit in the first network unit with the second network unit is no longer needed.

The invention provides the advantage that further clock sequences can be selected at a later time without settings or changes to the firmware in the first network unit and bus operation between the first and second network unit does not need to be interrupted in this case.

Further special features of the invention can be seen in the explanation for the Figures of an exemplary embodiment with reference to schematic drawings.

The figures show:

Figure 1 a block diagram for clock synchronization,
Figure 2 a block diagram of a clock recovery unit,
Figure 3 a block diagram of a further circuit for clock synchronization,
Figure 4 pulse diagrams,
Figure 5 an embodiment of a bus signal PWDC,
Figure 6 pulse diagrams for forming a safety margin between the clock signals of different channels,
Figure 7 incorporation of blocking areas,
Figure 8 block diagram of an N-channel decoder,
Figure 9 the associated pulse diagram,
Figure 10 an associated mask layout,
Figure 11 a pulse distance algorithm for a 3-channel and
Figure 12 for a 4-channel bus signal.

Figure 3 shows a schematic layout of a circuit for clock synchronization. This circuit of an interworking unit NUE is formed from a first network unit NTDM and a second network unit NP. The first network unit is divided up into one or more bus signal provision units CH1,...,CHn. The second network unit NP features a network unit system controller NPSS as well as a packet hub PHUB, with for example firmware FWM, a decoder unit DE with a decoder control unit DS as well as a clock generator unit T typically embodied with a Phase-Locked Loop unit PLL being arranged in the packet hub PHUB. The bus signal provision unit CH1,...,CHn can preferably be realized in a HW module and be adapted by configuration to the properties of the network environment by the operator. Redundant circuit units and associated connecting paths are not shown. The corresponding reference clock signals RCLK are recovered in the clock recovery unit CR from the data signals DSE1,...,DSEn present on the input side at the bus signal provision units CH1,...,CHn and forwarded in each case to a channel encoder KK1,...,KK4 which operates separately. These reference clock

signals can also be referred to as clock source in each case. In a first step a reference frequency f(REF) is created by frequency division in the channel encoder from the reference clock signal RCLKi present on the input side in each case. In a second step the created reference frequency f(REF) is encoded with the aid of the reference clock signal RCLK into a channel signal KS. Based on a pre-selection which can be set in the configuration register KR, a bus signal PWDC is formed from the individual channel signals $KS_1,...,KS_n$ via s summation signal generation unit SB and forwarded to a bus driver BT. A bus signal PWDC is forwarded to the decoder unit DE of the second network unit NP via the first connection REFBUS.

This circuit arrangement as shown in Fig. 3 provides the advantage that the opportunity exists here for creating all pre-selected reference clock signals RCLK1,...,n from a single clock recovery unit CR or individual reference clock signals from the different bus signal provision units CH1,...,CHn and transmitting them to the second network unit NP. Data signals DSEn with suitable clock quality can be selected through configuration by the network operator.

A reference clock signal RCLKn is selected in the second network unit NP for a synchronization according to a priority list which can be defined in the network unit system controller NPSS of the second network unit NP. In the event of a fault, the decoder unit DS is used to help effect a delay-free switchover to another, possibly also higher-priority clock quality without involving the circuit units in the first network unit NTDM in connection with the network unit system controller NPSS of second network unit NP. The network unit system controller NPSS in the second network unit NP is notified immediately by the decoder DE about faults, such as for example a failure of the reference clock signal

RCLK1,...,RCLKn. The failed reference clock source RCLK1,...,RCLKn is assigned in the network unit system controller NPSS on the basis of the stored configuration data.

The advantage of this circuit and the associated method in accordance with Fig. 3 lies in the fact that the firmware module in the first network unit NTDN and also a synchronization of the selection processes in the interface units is dispensed with. A further advantage lies in the fact that the further reference clock signals RCLKn can be selected at a later time without reconfiguring the first network unit NTDM and interrupting the bus operation between the network elements. This brings with it an increase in flexibility for the network operator so that changes in his network environment or expansion measures for his networks can be undertaken at any time.

The formation of the bus signal in the bus signal provision unit CHn is described below.

The formation of the bus signal PWDC is explained in greater detail below with reference to the diagrams in Fig. 4 and 5. The individual channels signals KSi, KSj are generated directly from the recovered reference clock signals RCLK by a frequency reduction and encoding, in that for each channel in each case with the periodicity of the defined reference frequency f(REF) a number of pulses corresponding to the total number of channels is created and for each channel the pulses are allocated fixed pulse distances di, dj. The pulse distances can be equidistant distances or freely selected distances. The pulse distances are also referred to as distance parameters. In accordance with the diagram in Fig. 5 the equidistant pulse distances of the individual channels KSi, KSj are embodied differently.

Within the individual channels different pulse widths are formed to identify the phase distance to the reference source (rising edge of the reference frequency f(REFx)). The pulse widths can for example be embodied with a linear gradation. It is advantageous for the pulse widths of the pulses to be embodied in ascending order for the pulse sequences. A unique assignment of the channels KS1,...,KSn in the bus signal PWDC is given by the defined pulse distances and pulse widths.

The pulse width of the pulse $PW_1,...,PW_k$ is based on a quantizing of the bus signal PWDC. The quantizing of the bus signal PWDC is defined by the pulse width of the RCLK reference clock signals. A phase relationship of the relevant reference frequency f(REFx) through the leading edge of the first pulse of the channel signal KSx (reference source) enables a channel selection in the decoder DE of the second network unit NP.

The pulses of the channel signals KS1,.....,KSn are logically ORed with each other in the bus signal PWDC in negative logic (low-active), see Fig. 5. The distance parameters within the individual channels are dimensioned so that between the pulses there is still a sufficient safety margin S, as shown in Fig. 6, between the individual pulses.

As a result a frequency offset caused by jitter or wander or plesiosynchronicity between the independent clock sources RCLK1,...,RCLKn there is a slight phase shift of the pulses of the channel signals KS1,...,KSn originating from different channels. Specifying the distance parameters di,...,dj enables at least one pulse from the channel signal KS1,...,KSn of each channel to be transmitted without a collision and allows it to be used for synchronization of the central PLL in the clock generation unit T of the second network unit. Each individual

pulse in the channel signal KS1,...,KSn has a defined phase relationship to its reference source through its predefined pulse width PW1,...,PWn. The PLL in the clock generation unit T can thus operate synchronously without adverse effects despite a collision-related change of the phase position of the selected pulse sequence. In the case of a collision in the selected impulse sequence the PLL can access a plurality of the redundant pulses in the channel signal with the aid of the control logic DS in the decoder DE and on the basis of the defined pulse width can execute a phase correction corresponding to the channel-specific distance parameters, in order to undertake a seamless transition.

With reference to a tabular listing, as presented in Fig. 11 and 12 as well as in the pulse diagrams of Fig. 6 and 7, a definition of the pulse distances di,...,dj for the bus signal PWDC with a 3- and 4-channel system is specified. The resulting figures relating to the phase position in Fig.11 are explained in Fig. 7. The channel signals KS1, KS2, KS3 are also referred to below as channels K1, K2, K3.

Arranged in a starting position (phase 0) is the rising edge of the first pulse with the pulse width PW1 in the channels K1, K2, K3. The phase position is specified in the phase units corresponding to the quantizing q of the reference clock signal RCLK. In the example q=61ns and corresponds to a half period length of the 8192Khz reference clock signal RCLK. The pulse widths PW1=q, PW2=2q, PW3=3q are embodied in accordance with a linear classification.

A blocking area SBR ensures a sufficient safety margin between the individual pulses below the channel signals with the aim of detecting a collision with the pulse sequence selected from the clock generation unit in good time and initiating a

switchover with the aid of the control logic to an undisturbed pulse sequence in a new phase position in the channel.

The distance parameters d1, d2, d3 as also shown in Fig.6, which can also be referred to as pulse distances of distance parameters are selected with regard to maintaining a possible reference clock signal, in that the blocking areas SBR of all channels involved are also taken into account. The controlling thus created for a scheme for concatenating pulses with blocking areas SBR can be defined by the subsequent algorithm (see Fig. 11, 12):

Bus signal with 3 channels	Bus signal with 4 channels
max. pulse width PW3 = 3*q	. pulse width PW4 = 4*q
	d1 = 3*(2n+1)
d1 = 2*(2n+1)	d2 = 4*(2n+1)
d2 = 3*(2n+1)	d3 = 5*(2n+1)
d3 = 5*(2n+1)	d4 = 7*(2n+1)

In these formulae n is a factor for the blocking area SBR, which ensures a sufficient safety margin between the pulses of the bus signal PWDC. The factor n has the phase unit q. The value of n is varied as a function of the number of channels and the associated maximum pulse width, in order to obtain a sufficient safety margin S, as shown in Fig. 6.

For secure processing in the decoder DE with only double the clock rate, the safety margin corresponding to the pulse diagram should amount to at least S=2*q. With this procedure the decoder DE can work directly with the clock frequency of the PLL quartz oscillator in the clock generation unit T of 32,768MHz. With the above algorithm this requires a blocking area SBR of n=4*q for a 3-channel system or n=5*q for a 4-channel system A prerequisite is a sufficient bandwidth for a distortion-free pulse transmission of the bus signal PWDC for

the selected quantizing q of the reference clock signal.

The algorithm is illustrated below in a pulse diagram with reference to the 3-channel system in Fig. 7. To simplify an optimization only the maximum pulse width PW3 is considered, with greater safety margins than necessary thus being produced for pulses with smaller pulse widths. Taken as a reference position for this is the initial phase position of the first pulse of the channels K1, K2, K3 and the leading pulse edge in each case (phase 0). The blocking area SBR $\pm n*q$ is related to the rising edge of the subsequent pulses. According to the algorithm the distance parameter d1 in the first channel of the 3-channel system amounts to $d1=18*q$, so that the first blocking area SBR of the first channel K1 begins on the phase position axis at $14*q$ and ends at $22*q$. Immediately after this the blocking area SBR of the second pulse PW2 of the second channel K2 begins at $23*q$, so that there is no gap between the blocking areas. Only before the last blocking area around the rising edge of the third pulse PW3 in the third channel K3, because of the equidistant pulse distance definition, is there a gap of $28*q$ (no longer shown in Fig. 7).

In accordance with the formula $[q*(3*d3+n)]-1$ the maximum achievable reference frequency f(REF) in the 3-channel system amounts to 118KHz, assuming a quantizing of q=61ns (see Fig. 11). For application of binary division relationships (2n) this produces a limitation of the reference frequency f(REF) to be transferred into the bus signal to 64kHz. Under the same conditions this value reduces in the 4-channel system to 32kHz, see Fig. 12. With a greater number of channels the equidistant pulse distance definition can be abandoned to counter too great a limitation of the achievable reference frequency.

An exemplary embodiment for encoding and decoding of the bus signal PWDC is shown in Figures 3 and 8 as well as in the pulse diagrams 9, 10 belonging to Fig. 8.

The channel signals KS1, KS2, ...,KSn are generated in the encoding part KK of the bus provision unit CH1,...CHn with the aid of binary synchronous counters which are clocked directly from the reference signals RCLK. In accordance with the diagram shown in Fig. 3 the distance and pulse width parameters are defined separately for each channel through configuration data and created with combinational networks. The clock recovery unit CR only enables and forwards to the encoder KK the intended reference clock signals RCLKn. If there is a loss of quality, enabled reference clock signals RCLKn are deactivated in good time by the clock recovery unit CR as a result of an alarm module integrated into this unit. After the channel signals KS1,...,KSn have been merged, the sum signal is routed via tristate bus drivers and transmitted to the REFBUS as a bus signal PWDC.

The mode of operation of a decoder DE in the second network unit NP is explained with reference to the basic circuit diagram in Fig. 8. The decoder DE is subdivided into other units, including functional blocks KSY, KSK and MST. These functional blocks are a channel synchronizer KSY, a channel selector KSK and a mask controller MST. All functional blocks are connected to the control unit DS. Three independently-operating channel separators KSP1,...,KSPn are arranged in the channel synchronizer KSY, corresponding to the number of channels. The channel signals are filtered out from the bus signal with the aid of a digital regulation circuit in a channel separator KSP in the channel synchronizer KSY function block. To this end the pulse width filters PWF or channel-specific pulse-distance filters PDF are employed for the

correct selection and for the maintenance of the synchronism in the channel synchronizer. All these functions are executed as mask functions, so that a real-time transmission of the reference signals up to the clock generation unit T in an unrestricted bandwidth in the decoder is made possible.

The first line of the pulse diagram in Fig. 9 shows the signal sequence transmitted on the bus. The output signals of the channel separators are reproduced in the subsequent pulse diagrams. Since the channel signals are not exactly synchronous with each other, the synchronization requires three independent control circuits for the three channels.

A switchover between the simultaneously available reference clocks available in the channel synchronizer KSY is undertaken on the basis of a list of priorities in the channel selector module KSK stored in the control unit DS. This allows a fast HW-controlled reaction to the problem.

The pulse sequence PW1, PW2, PW3 of a channel signal Kn selected in the channel selector module KSY is given a synchronously maintained mask in the mask control block MS, with for each reference clock period f(REF) only one collision-free pulse is forwarded to the PLL. In accordance with diagram shown in Fig. 10 this mask is adapted to the pulse width classification of the channel signal, with the mask being subdivided into at least two areas, the pass-through area DLB and the control area KLB. The pass-through area DLB is enabled prioritized in accordance with pulse width classification, if a number of collision-free pulses were found in the channel signal. The narrowest pulse is assigned the highest priority since it contributes directly to the phase position of the reference source.

The control area KLB is the outer part of the mask and is

responsible for a collision prediction. If a foreign pulse from any given side comes into the control area KLB the pass-through area DLB of the mask involved is then blocked and simultaneously the next collision-free mask is enabled. The control area KLB is 2UI wide, with the abbreviation UI standing here for a Unit Interval and relating to the system clock period of the decoder. By comparison with the quantization stage used in the encoder, because of the doubled clock rate used, q stands here for a UI=0.5*q (31ns), this corresponds to a system clock of 32,768MHz.

The safety margin SBR of SBR=2*q parameterized in the algorithm is thus made up of a reserve area of 1*q(=2UI) for the pass-through area DLB, as well as of a further 1*q(=2UI) for the control area KLB of the mask. The digital regulation in the channel synchronizer operates with an internal quantizing of one UI, so that in the pass-through area in addition to quantization jitter, one UI remains reserved for the residual jitter on the channel signal. The quantizing of the pulse width measurement or the collision detection for the control area can on the other hand, with the use of the double sampling rate of 0.5UI, be undertaken using both switching edges of the system clock, which increases the security and the dynamics of the regulation.

The blocking and enabling of the masks in different phase positions within a selected reference clock path is undertaken with the aid of a phase adaptation circuit. In units of the known channel-specific distance parameter a phase adaptation is performed here at each mask change. In this way pulses selected for synchronization always arrive in the same phase position as seen by the PLL.

For PLL modules of which the phase detector, e.g. an EXOR

circuit, does not operate with edge control, the pulse width is also regenerated here after masking, by a sampling ratio of 1:1 being set digitally.

With digitally regulated mask control the pulses of the reference signals are forwarded without intermediate processing, meaning in real time to the PLL. The masks merely serve to filter out the redundant pulses within a channel.

All functions of the mask control can be executed in hardware in order to achieve optimum dynamics for the regulation. Individual functions of the mask control can also be relocated by corresponding software into the firmware module FWM of the packet hub PHUB. The possible longer reaction time arising as a result can be bridged by possible provision of a holdover function in the Phase-Locked Loop circuit PLL.

The channel selector module KSK can also be integrated into the module for mask control MST by corresponding enabling of the pass-through masks. Furthermore the formation of the mask area, control and pas-through area can be linked directly to the digital regulation circuit of the channel synchronizer. The phase adaptation circuit can be implemented in the PLL feedback loop in a common hardware embodiment.